Automotive, IoT Driving New Semiconductor IP and Compliance Requirements

Synopsys

ABSTRACT

The stringent design requirements for automotive and IoT system-on-chips is requiring the industry to adopt advanced process technologies such as TSMC's 16-nm and 7-nm to meet performance, power and area (PPA) targets. Moving to these FinFET processes has significant implications on physical IP design. In addition, recently a common area has been defined in terms of functional and operational safety compliance for automotive and IoT systems. IoT is typically categorized under IEC 61508. Automotive falls under the same umbrella with IP providers needing to ensure that their products meet stringent automotive standards such as ISO 26262 functional safety, AEC-Q100 reliability testing and TS 16949 quality management. It is clear that both physical and soft IP are impacted by market segmentation with regards to process technology and compliance.

This presentation will discuss the technical specifications for automotive and IoT designs with respect to physical (USB, PCI Express, DDR) and foundation IP. This will include how Synopsys has collaborated closely with TSMC to address the impact of aging/reliability such as HTOL, EM, TDDB, NBTI for physical IP on TSMC FinFET process technologies. The impact of the compliance requirements for these two market segments will also be presented for soft IP such as the addition of functional safety diagnostics.

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Silicon to Software

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Navraj Nandra

Automotive And IoT Worlds Merging

ADAS for Safety of Vehicles and Factory Systems (IoT Systems)

Safety Standards Bodies
- ISO
- IEC

Safety Standards Specifications
- ISO-26262 (Automotive)
- IEC-61508 (Industrial)
- ISO-60730 (Household)

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Impact On FinFET Process

Functional And Operational Requirements

IP Design Solutions For Physical IP

Summary

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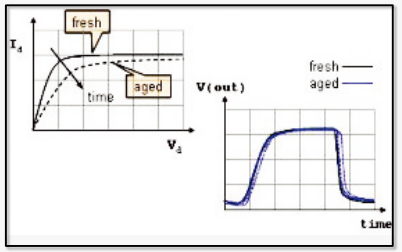
Transistors Do Age…Like Humans

- Transistors slow down over time
- Rate of aging very related to stress
- Similarities exist in the cause and effect of aging



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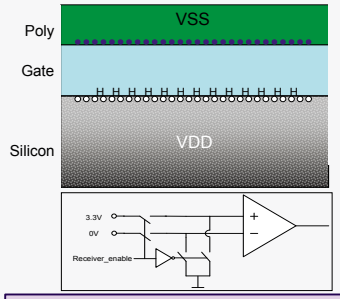
Different Aging Phenomena

- **NBTI**
  - Transistor holds same data for long periods
  - *"All work and no play"*
- **HCE**
  - Related to amount of switching
  - *Moving back and forth between jobs*
- **Oxide Breakdown**
  - Breakdown of gate-oxide between semi-conductors slowly over time
- **Electro-Migration**
  - Electron flow in same direction
  - *Blood flow*



Mitigation of the NBTI problem:
Introduction of symmetric stress on both inputs to the differential pair by pulling input to the same voltage during suspend mode.

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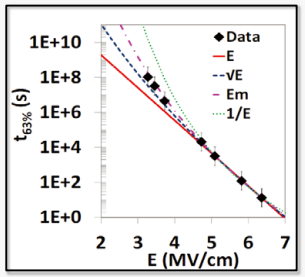
Reliability Concerns @ 7nm

- **HCI, NBTI, PBT…more of the same**
  - Significant progress in NBTI in second generation of finFETS
  - HCI slightly worse with higher fields,…. Lower VDD helps
  - PBTI in finFET: can ignore
- **TDDB…a growing problem**
  - Low-k: tighter metal pitches → higher "C" + higher E → need lower ϵ → more porous → weaker oxide → worse TDDB
  - TDDB also impacts gate oxide: high-k
  - Statistical in nature
  - No unified model



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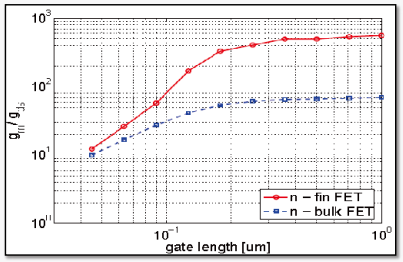
Impact On Design - Schematics

Schematics, Electrical Parameters

- **Drive** similar for PMOS/NMOS
- **Device** matching better
- **High speed blocks** needed
- **Aging simulation** important
- **Smaller devices** get hot
- **New tools** for EM, IR, full RCC sim
- **In house ESD** a must



g_m/g_{ds} of bulk and FinFET

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Impact On Design – Layout

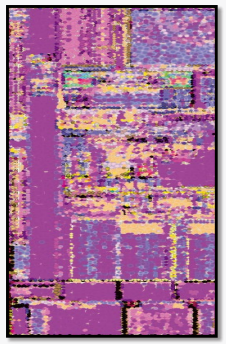
Layout Changes

Increase of redistricted design rules

- The lowest-layer metals only go in one direction
- Routing non-preferred orientation is more difficult
- Arrays of long length devices are not allowed

Active layers shrink more than metal interconnect

- Compacting transistors too much mean signals in hierarchy cannot be connected
- Prepare routing channels and then fill devices around the routes



7-nm USB 2.0 PHY

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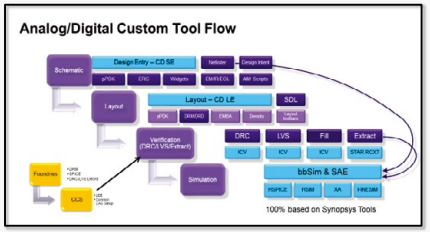
Impact On Design - Methodology

- **System Level**
  - Simulate **performance** of TX , Rx, CDR circuitry
  - Include xtalk, jitter, channel impairments
  - Performance sims – JTOL, RX eye margin
- **Extracted simulation**
  - Capture extracted device parameters (ie. STI, WPE, etc…)
  - RCC - capture full parasitic and IR drop
- **Variability**
  - Monte Carlo simulations, Sigma Amplification
- **Supply Sequencing**
  - Power supply noise; collapsing and ramp sequences
  - Leakage and floating nodes checked



- **Leakage Tests**
  Leakage measurement - power down blocks and measure currents in IDDQ and power collapse modes
- **IR drop**
  -5%+ extra 50 mV drop headroom corner sim. to check for basic functionality even with excessive IR drop

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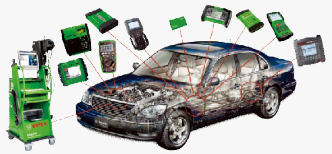
Hardware Requirements To Enhance Functional Safety For IoT & Automotive

- **Write protection** in Elastic Buffers
- **EDC protection** on headers
- **Parity protection on d**atapath - using byte parity
- **Parity protection on configuration** registers
- **Protection on write/read** into memories
- **Concatenate state registers** with parity check
- **Key module redundancy** for error handling & elastic buffers
- **Triplicate registers** with voting logic
- **System informed of errors** via various dedicated interrupts
- **One hot state machine** protection for bad States

Operational Requirements For Automotive & IoT

Recommended Self-Diagnostics Tests

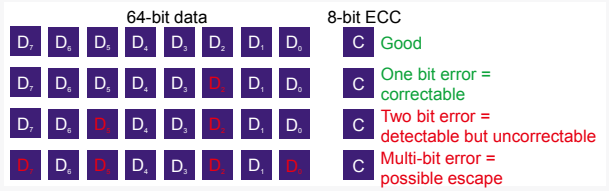
- **Recommended self-diagnostics tests**
- **CPU diagnostics**
  - –CPU Registers
  - –CPU clock accuracy & frequency
- **Memory diagnostics**
  - –NVM
  - –SRAM
- **Other**
  - –Watchdog timers
  - –Diagnostics of interrupts
  - –Diagnostics of stack overflow and/or underflow
  - –Diagnostics of algorithm variables



Adding RAS Features To PCIe, DDR Controllers

Reliability, Accessibility, Serviceability

- **Implement data protection** (parity, ECC) in conjunction with protocol defined mechanisms to detect and correct errors in the data path and RAMs
- **Use event counters** and statistics to monitor system availability
- **Leverage error injection** & silicon debug capabilities to diagnose issues, validate system recovery



Using ECC for multi-bit error detection

Reference Synopsys [4]

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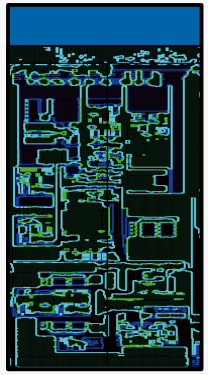
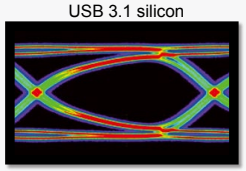
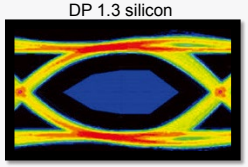
7-nm Proof Points: USB 3.1 PHY (Type C)

Lowest Power, Smallest Area







- **Protocols:** USB3.1 / DP
- **Data Rate:** 5G / 10G
- **Area:** 30% smaller than 10FF
- **Lane:** x2 available for Type-C
- **Loss:** >25dB @ 5 GHz
- **EQ:** DFE, CTLE, FFE

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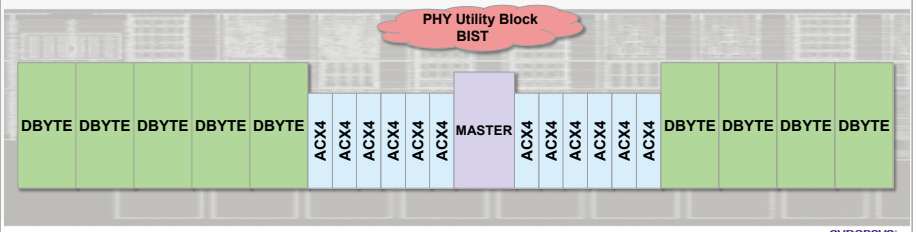
7-nm Proof Points: LPDDR4 PHY 4267 Mb/s

- **DRAM on PCB**, UDIMM, SODIMM
- **Processor** based training
- **4 trained** states/frequencies
- **VT compensated** delay lines
- **IO equalization**
- **Flexible orientation** including “L”



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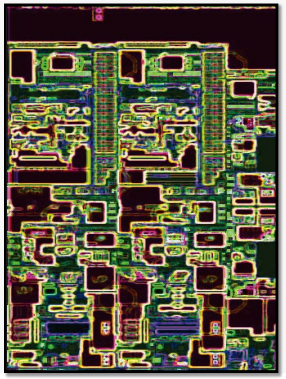
7-nm Proof Points: PCIe 4.0 PHY

- **Power:** 30% lower than 16FF
- **Area:** 30% lower than 16FF
- **EQ:** DFE, CTLE, AGC, FFE
- **Performance:** > 29 dB @ 8 GHz
- **Core** = 0.75 V; **I/O** = 1.5 V or 1.8 V
- **Key features:**
  - P1.1/2, SRIS
  - REFCLK repeater
  - Bifurcation/aggregation



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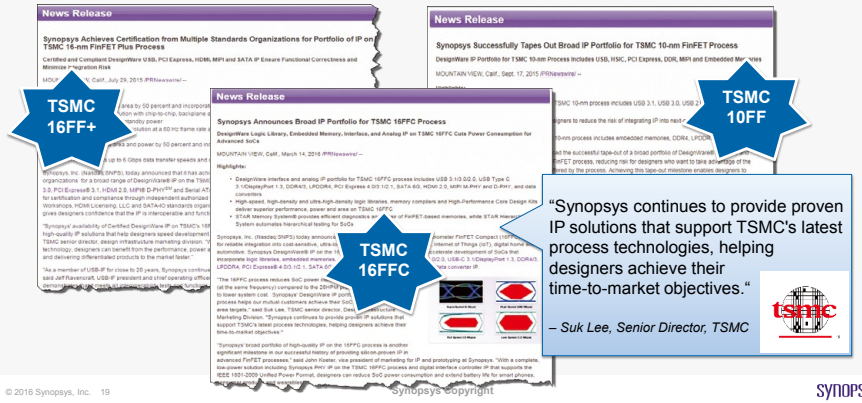
Synopsys & TSMC Collaboration To Achieve Best PPA In 10/16-nm FinFET Processes



Summary

- Automotive and IoT SoCs require TSMC's 16-nm and 7-nm process to meet PPA targets
- Functional and operational safety compliance is required
- IP designed for ISO 26262 functional safety, AEC-Q100 reliability testing, TS 16949 quality management is critical
- Foundry partnership is a key to success – TSMC OIP